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# United States Patent [19]

Wincn

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## [54] BI-PHASE DECODER PHASE-LOCK LOOP IN CMOS

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**Related U.S. Application Data**

[63] Continuation-in-part of Ser. No. 480,426, Feb. 15, 1990, and a continuation-in-part of Ser. No. 595,068, Oct. 10, 1990, Pat. No. 5,164,960.

[51] **Int. Cl.**[5] ..... **H03D 3/24**

[52] **U.S. Cl.** ..... **375/120**; 375/119; 331/1 A

[58] **Field of Search** ..... 375/81, 82, 97, 106, 375/119, 120; 331/1; 328/63, 72; 455/260, 180

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[57] **ABSTRACT**

A bi-phase decoder for extraction of an embedded clock in a Manchester encoded signal operating at about ten megahertz. A phase-lock loop (PLL) includes a phase frequency detector and an interruptible voltage controlled oscillator (VCO). The PLL has a narrow bandwidth for stability to reduce effects of five megahertz components on clock extraction. The bi-phase decoder has a fast acquisition time to ensure frequency and phase lock during a preamble portion of an input data packet. A clock reference operates the PLL and the VCO at a nominal frequency of the embedded clock. Receipt of a data packet initiates interruption of the VCO operation to switch in the received data. The VCO resumes operation in phase with the received data packet and at about the proper frequency, therefore acquisition is fast. The VCO is designed to resume operation after operation at a particular phase to help in phase alignment.

**7 Claims, 7 Drawing Sheets**