

**JOHN M. WINCN**

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**MIXED-SIGNAL AND SERIAL I/O (FOR SYSTEM LEVEL & SIGNAL INTEGRITY, SEE BELOW):**

**Aug 2009 – Sep 2010** **Numetrics Management Systems, Inc.** (Direct contract, Analog & Mixed Sig)  
20863 Stevens Creek Blvd., Suite 510, Cupertino, CA 95014  
<http://www.numetrics.com/aboutus/>  
Main: 408-351-5800

- I delivered Effort and Time-to-Complete estimates related to Mixed-Signal Analog projects, for ultimate use in NMSI product-development planning software
- Development forecasts considered mature and fine-geometry technology

**Apr 2006 – Present** **University of California, Santa Cruz** (Staff, then graduate student)  
**Baskin School of Engineering, Graduate Research**  
1156 High St., Santa Cruz, CA 95064-1077  
<http://www.soe.ucsc.edu/>  
Voice: 831-459-1035 (no voicemail), Email: [jmwincn@soe.ucsc.edu](mailto:jmwincn@soe.ucsc.edu)

- Working on completion of PhD, Optic Data Communication over Polymer Optic fiber
- BiCMOS and CMOS circuit design, Polymer Optic Fiber links
- 1 – 10 GBd Serial line drivers/receivers (Electric-Optic, Optic-Electric)
- National Semiconductor (TI) 180nm CMOS, 250nm and 130nm BiCMOS
- Cadence Virtuoso, Agilent ADS, Matlab
- Responsible for periodic research reports
- Acted as SoE Contact between the university and National Semiconductor (now a division of Texas Instruments, Inc.)

**Mar 2006 – Jan 2007** **NxP Semiconductors, Inc.** (formerly Philips Semiconductors)  
411 E. Plumeria Drive, San Jose, CA 95134-1924, <http://www.nxp.com>  
(Was: 1109 McKay Dr., San Jose, CA 95131-1706)

- Contract Analog circuit design, Medical systems components
- I was responsible for feasibility and design of Analog I-to-F convertors (X-Ray Detection), using Cadence Virtuoso and Matlab
- 180nm CMOS technology

**Oct 2001 – Mar 2005** **Toshiba America Electronic Components, Inc.** (through a contract service)  
2590 Orchard Parkway, San Jose, CA 95131  
Main: 408-526-2400, Fax: 949-526-2410 <http://www.toshiba.com/taec>

- Contract circuit design, Line Driver and Receiver cell library
- PCI-X 1, PCI-X 2.0a, 133MHz to 533MHz; 90nm CMOS
- I completed initial circuit design with Cadence Virtuoso and Synopsys Hspice in less than 6 months
- I was responsible for project reports, design review notes, application notes, and end-user notes

**Nov 1998 – Oct 1999**    **Transcendata, Inc.** (Serial Optic Transceivers, ceased operation 1999)  
1029 Corporation Way, Palo Alto, CA 94303-4305

- Principal Analog Design Engineer
- I was responsible for design and development of physical layer interface for PAM-5 Optic Serial Data Communication using Cadence Analog Artist and Matlab
- Wrote a preliminary product specification for the proposed SERDES
- Target design 180nm CMOS, TSMC

**Apr 1988 – Jun 1997**  
**Feb 1978 – Sep 1986**

**Advanced Micro Devices, Inc.**

One AMD Place, P.O. Box 3453, Sunnyvale, California 94088-3453  
Main: 408-749-4000, <http://www.amd.com/us/aboutamd/>

- Member of Technical Staff, Network Products Division, CMOS Analog Circuit Design
- Voting member, IEEE Computer Society's 802.3 10BaseT Task Force
- I completed design and development of CMOS PLL, Line drivers, Receivers, 10b ADCs, 12b DACs, Opamps, Band-Gap References, Single-Integration Delta-Sigma Modulator
- Design tools included Hspice, Mentor Design Architect, MathCad

I completed design and development work for the physical layer in all of the following products (either 0.35 $\mu$ m or 0.25 $\mu$ m CMOS):

- 200Msps DAC for 10BaseT/100BaseT
- AM79C98 Twisted-Pair Ethernet Transceiver (TPEX)
- AM79C980 Single-chip Integrated Multiport Repeater for 10BaseT (IMR)
- AM79C900 Serial Interface Adapter (SIA) for Single-chip Integrated Local Area Communications Controller (ILACC)
- AM79C30 "S" Interface Digital Subscriber Controller (DSC), Voice CODEC
- AM7901, AM7905 NMOS Subscriber-Line Audio processing Circuit (SLAC)
- AM7910, AM7911 NMOS Single-chip 1200 Baud FSK modems
- I was responsible for Analog design review notes and product Engineering notes; I sometimes worked directly with Product Engineering and Product Marketing
- Our design and development team grew AMD's network product line from ~\$20M in the late 1980s to ~\$250M annual revenue in the mid 1990s.

**Sep 1986 – Apr 1988**    **Level One Communications, Inc.** (Now a division of Intel)  
105 Lake Forest Way, Folsom, CA 95630

- I was responsible for initial design of CCITT (Now ITU) I.430 Line drivers and Receivers (ISDN), using AMI

#### **SYSTEM LEVEL, SIGNAL INTEGRITY, BOARD DESIGN:**

**Jun 2000 – Oct 2001**    **Atoga Systems, Inc.** (DWDM Routers; sold to Arris, Inc., 2003)  
49026 Milmont Drive, Fremont, CA 94538, 510-687-9700

- Member of Technical Staff – Hardware Design and Photonics
- I was responsible for OC-48 Line Card development, as related to signal

integrity issues and wireline RF over FR-4

- Team member for development of WDM line card with fast tunable lasers
- Team member for OC-192 product development
- I was responsible for development of Sonet-compatible CDR (Proprietary ASIC development work)

**Jul 1997 – Nov 1998**

**G2 Networks, Inc.** (Storage Area Networks, ceased operation 1999)  
16780 Lark Ave., Los Gatos, CA 95032-7646

- Senior Analog Engineer
- I was responsible for on-going development of BiCMOS SERDES ("Bluejay"), 1.0625GBd OOK (1.25GBaud capable)
- Design tools included Hspice, Cadence Analog Artist
- I acted as in-house contact for: development of a Honeywell VCSEL module; contact with TSMC foundry; outside silicon test

**Jun 1975 – Feb 1978**

**Applied Technology, Inc.** (Once a division of Litton)  
P. O. Box 7012, San Jose, CA 95150-7012

- Design Engineer, Secret Clearance
- I was responsible for development of 4-Bit 50MSPS Bipolar Flash ADC, for Radar Homing/Warning Receiver
- Team member, development of 1MHz Manchester 1553 line driver with active tri-state output (Hybrid module)

#### **MEMBER OF IEEE ENGINEERING SOCIETIES:**

Solid-State Circuits  
Signal Processing  
Microwave Theory and Techniques

#### **EDUCATION:**

**Sep 2007 – Present**

**University of California, Santa Cruz**  
**Baskin School of Engineering**  
1156 High St., Santa Cruz, CA 95064-1077

**Sep 1972 – Jun 1975**

**California Polytechnic University** BSEE, 1975  
3801 W. Temple Ave., Pomona, CA 91768-4005

#### **GRANTED U. S. PATENTS**

1. Pseudo-AUI Line Driver and Receiver Cells for Ethernet Applications; J. M. Wincn; No. 5,694,427, Dec 1997
2. High Speed, Low Power CMOS D/A Convertor for Wave Synthesis in Network; J. M. Wincn; No. 5,600,321, Feb 1997
3. High Speed CMOS D/A Convertor for Wave Synthesis in Network; J. M. Wincn; No. 5,592,166, Jan 1997
4. Reversible AUI Port for Ethernet; J. M. Wincn; No. 5,568,515, Oct 1996
5. Bi-Phase Decoder Phase-Lock Loop In CMOS; J. M. Wincn; No. 5,276,716, Jan 1994
6. Method and Apparatus for Squelch Circuit in Network Communication; J. M. Wincn, et. al; No. 5,327,465, Jul 1994
7. Method and Apparatus for CMOS Differential Line Driver Having a Rapid Turnoff; J. M. Wincn; No. 5,263,049, Nov 1993

8. Automatic Polarity Detection and Correction Method and Apparatus; John M. Wincn, et. al; No. 5,257,287, Oct 1993
9. Medium Attachment Unit for Use with Twisted Pair LAN; John M. Wincn, et. al; No. 5,164,960, Nov 1992
10. CMOS-Transistor-Based Digital-to-Analog Converter; J. M. Wincn; No. 4,635,038, Jan 1987
11. Sampling Comparator Circuit for Processing a Differential Input; John M. Wincn, et. al; No. 4,542,308, Sep 1985

**COMMUNITY SERVICE**

In an effort to share my technical expertise, I applied and was appointed to the Cupertino Telecommunications Advisory Commission, City of Cupertino, in Feb 1991 and again in Feb 1995. I served as chairman for three consecutive years. The commission's primary responsibility was to review and forward comment or advice to the City Council on technical issues that were related to operation of Cable Television service within the City of Cupertino. The committee's secondary responsibility was to accept comments from residents that were related to local Cable TV service and respond or forward comments to the City Council.